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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,322	12/27/2001	Seiichi Nakatani	10873.860US01	9631

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EXAMINER

CHU, CHRIS C

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 06/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/033,322

Applicant(s)

NAKATANI ET AL.

Examiner

Chris C. Chu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 April 2003.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 - 12 and 23 - 42 is/are pending in the application.
- 4a) Of the above claim(s) 4, 6 - 9, 23, 24 and 27 - 34 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 - 3, 5, 25, 26 and 37 - 42 is/are rejected.
- 7) ☒ Claim(s) 10 - 12, 35 and 36 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All   b) ☐ Some \*   c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)                      4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)                      5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_                      6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Response to Amendment***

1. Applicant's amendment filed on April 3, 2003 has been received and entered in the case.

***Election/Restrictions***

2. Claims 4, 6 – 9, 23, 24 and 27 - 34 continue to be withdrawn from consideration for the reasons provided in the Office action mailed on December 4, 2002.

On page 9, applicant argues “applicants submit that claims 6 – 8, 27 – 29 and 30 – 32 are within the scope of currently pending generic claims and therefore should be retained and reinstated if generic claims are allowed.” This argument is not persuasive because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

*Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1 ~ 3, 5, 25, 26 and 37 ~ 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatani et al. in view of Hirai et al.

Regarding claim 1, Nakatani et al. discloses in Fig. 5 and column 11, lines 23 ~ 35 a component built-in module comprising:

- a core layer (f) formed of an electric insulating material; and
- a plurality of wiring patterns (506) formed on at least one surface of the core layer;

wherein:

- the electric insulating material of the core layer is formed of a mixture comprising at least an inorganic filler and a thermosetting resin;
- at least one selected from the group consisting of active components (504) and passive components (505) is contained in an internal portion of the core layer;
- the core layer has a plurality of wiring patterns (506) and a plurality of inner vias (501) formed of a conductive resin; and
- the electric insulating material formed of the mixture comprising at least an inorganic filler and a thermosetting resin of the core layer.

Nakatani et al. does not disclose an electric insulating layer formed on at least one surface of the core layer; the core layer and the electric insulating layer are formed of different electric insulating materials; and the core layer has a modulus of elasticity at room temperature in the range from 0.6 GPa to 10 GPa. However, Hirai et al. teaches in Fig. 7 and column 7, lines 24 ~ 40 an electric insulating layer (70) formed on at least one surface of a core layer (4); the core layer and the electric insulating layer are formed of different electric insulating materials; and the core layer has a modulus of elasticity at room temperature in the range from 0.6 GPa to 10 GPa. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakatani et al. by using the electric insulating layer and the modulus of elasticity of core layer in the range from 0.6 GPa to 10 GPa as taught by Hirai et al. The ordinary artisan would have been motivated to modify Nakatani et al. in the manner described above for at least the purpose of preventing the IC module A from being inappropriately displaced in the receiving portion 72 (column 7, lines 63 ~ 66).

Regarding claim 2, Nakatani et al. discloses in Fig. 4, column 7, lines 4 ~ 16, column 9, lines 22 ~ 26, column 11, lines 53 ~ 63 and column 18, lines 15 ~ 19 a component built-in module comprising:

- a core layer (401a) formed of an electric insulating material; and
- a plurality of wiring patterns (402a) formed on at least one surface of the core layer; wherein:
  - the electric insulating material of the core layer is formed of a mixture comprising at least an inorganic filler and a thermosetting resin;

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- at least one selected from the group consisting of active components (403a) and passive components (403b) is contained in an internal portion of the core layer;
- the core layer has a plurality of wiring patterns and a plurality of inner vias (404) formed of a conductive resin; and
- the electric insulating material formed of the mixture comprising at least an inorganic filler and a thermosetting resin of the core layer; and
- the thermosetting resin comprises a plurality of thermosetting resins having different glass transition temperatures.

Nakatani et al. does not disclose an electric insulating layer formed on at least one surface of the core layer; the core layer and the electric insulating layer are formed of different electric insulating materials; and the core layer has a modulus of elasticity at room temperature in the range from 0.6 GPa to 10 GPa. However, Hirai et al. teaches in Fig. 7 and column 7, lines 24 ~ 40 an electric insulating layer (70) formed on at least one surface of a core layer (4); the core layer and the electric insulating layer are formed of different electric insulating materials; and the core layer has a modulus of elasticity at room temperature in the range from 0.6 GPa to 10 GPa. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakatani et al. by using the electric insulating layer and the modulus of elasticity of core layer in the range from 0.6 GPa to 10 GPa as taught by Hirai et al. The ordinary artisan would have been motivated to modify Nakatani et al. in the manner described above for at least the purpose of preventing the IC module A from being inappropriately displaced in the receiving portion 72 (column 7, lines 63 ~ 66).

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Regarding claim 3, Nakatani et al. discloses in Fig. 4, column 7, lines 4 ~ 16, column 9, lines 22 ~ 26, column 11, lines 53 ~ 63 and column 18, lines 15 ~ 19 a component built-in module comprising:

- a core layer (401a) formed of an electric insulating material; and
- a plurality of wiring patterns (402a) formed on at least one surface of the core layer; wherein:
  - the electric insulating material of the core layer is formed of a mixture comprising at least an inorganic filler and a thermosetting resin;
  - at least one selected from the group consisting of active components (403a) and passive components (403b) is contained in an internal portion of the core layer;
  - the core layer has a plurality of wiring patterns and a plurality of inner vias formed of a conductive resin; and
  - the electric insulating material formed of the mixture comprising at least an inorganic filler and a thermosetting resin of the core layer; and
  - the thermosetting resin comprises at least a thermosetting resin having a glass transition temperature in the range from -20°C to 60°C and a thermosetting resin having a glass transition temperature in the range from 70°C to 170°C.

Nakatani et al. does not disclose an electric insulating layer formed on at least one surface of the core layer; the core layer and the electric insulating layer are formed of different electric insulating materials; and the core layer has a modulus of elasticity at room temperature in the range from 0.6 GPa to 10 GPa. However, Hirai et al. teaches in Fig. 7 and column 7, lines 24 ~

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40 an electric insulating layer (70) formed on at least one surface of a core layer (4); the core layer and the electric insulating layer are formed of different electric insulating materials; and the core layer has a modulus of elasticity at room temperature in the range from 0.6 GPa to 10 GPa. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Nakatani et al. by using the electric insulating layer and the modulus of elasticity of core layer in the range from 0.6 GPa to 10 GPa as taught by Hirai et al. The ordinary artisan would have been motivated to modify Nakatani et al. in the manner described above for at least the purpose of preventing the IC module A from being inappropriately displaced in the receiving portion 72 (column 7, lines 63 ~ 66).

Regarding claims 5, 25 and 26, Nakatani et al. discloses in Fig. 4, column 7, lines 17 ~ 19, column 11, lines 23 ~ 35 and column 11, lines 53 ~ 63 comprising

- a core layer (401a) formed of an electric insulating material;
- an electric insulating layer (401b) comprising an electric insulating material formed of a mixture including an inorganic filler and a thermosetting resin, which is formed on at least one surface of the core layer; and
- a plurality of wiring patterns (402a) formed of a copper foil;
- wherein the core layer (402a) has a plurality of wiring patterns formed of a copper foil and a plurality of inner vias (404) formed of a conductive resin, and the wiring patterns are connected electrically to each other by the inner vias.

Regarding claims 37, 39 and 41, Nakatani et al. discloses in Fig. 4 the component being not built into the electric insulating layer provided on at least one surface of the core layer.



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Regarding claims 38, 40 and 42, Nakatani et al., as modified, discloses the glass transition temperature of the electric insulating material of the core layer being different from the glass transition temperature of the electric insulating material of the electric insulating layer provided on at least one surface of the core layer.

***Allowable Subject Matter***

5. Claims 10 ~ 12, 35 and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

The prior art of record does not teach or suggest, either singularly or in combination, at least a film-shaped passive component is disposed between the wiring patterns formed on at least one surface of the core layer.

***Response to Arguments***

6. Applicant's arguments with respect to claims 1 ~ 3 have been considered but are moot in view of the new ground(s) of rejection.

*Conclusion*

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu  
Examiner  
Art Unit 2815

c.c.  
June 9, 2003

A handwritten signature in black ink, appearing to read 'Eddie Lee', with a large, sweeping initial 'E'.

**EDDIE LEE**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**